SPECIFICATION

[Accurate junction capacitance model for high-speed circuit simulator]

Cross Reference To Related Applications

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Background of Invention

[0001]   In verifying the VLSI, especially in the circuit level, the speed and accuracy are the biggest research topics to tackle the complex and huge design, usually over tens of millions of transistors. There have been lots of researches to complete the design verification to meet the time-to-market, but the basic concept was that there are trade-off between speed and accuracy. In addition to the relation between them, the circuit level, verifying the VLSI at the transistor level, is facing the biggest difficulties among the levels of the design methodology, because the size of the transistors becomes too big to simulate in a day or in a week. To keep the simulation at the circuit level in a day or a week, a method of modeling of the MOSFET and an analysis technique to be applied at the circuit simulator are proposed. To overcome the conventional transistor level simulation, lots of techniques were devised. The table-lookup technique, which replaced the method of finding the value of characteristics of the transistor from time-consuming mathematic procedure, was popular because of its performance. The table look-up performs the simulation by searching the table that has all the characteristics of the transistor – such as temperature, current between drain and source of the transistor, Vgs, Vds, and the relation between them, etc. Among the characteristics, intrinsic capacitance of the MOSFET has the greatest effects on the high speed circuit simulator. Basically and conventionally, the value of the intrinsic capacitance is modeled as the value with the average, but it can have big

error impact on the circuit simulation because this technique cannot consider the variance of the capacitance depends on the Vsb or Vdb. To get more accurate simulation, division of the characteristic of the junction capacitance with value of the Vsb is proposed. Based on the value of Vsb, we divide small and large Vsb region, each region was represented by its region average value. By dividing it with regions, the value can have the bias dependant; the simulation with this idea can have accuracy as well as performance.

Brief Description of Drawings

[0002]   FIG. 1 is a simulation flow using lookup table modeling.

[0003]   FIG. 2 is a modeling junction capacitance of MOSFET

[0004]   FIG. 3 is the value of capacitance Cj1 at the small Vsb region , and The corresponding value at the large region is Cj2, and , which are modeled as Cj1, Cj2

Detailed Description

[0005]   *Procedure to generate lookup table of the MOSFET*

[0006]   *By parsing the input net-list, each of the transistors in the circuit was classified depends on the width and length of the transistors for spice-like simulator. Another words, the transistors were gathered depend on their size and template-set were built for the target simulator. With the template-set, the circuit simulator generates the lookup table, which the components of the tables are characteristics of the each transistors of the circuit. Template-set consists of template 1 and template 2. Template 1 has components to model the threshold voltage and the value of junction capacitance, while the template 2 has components to model the drain-source current and value of the gate capacitance of the transistor. The template in the Table 1 and 2 are the example for the HSPICE, the circuit simulator*

[0007]   *Table1. Sample template of HSPICE for a NMOS*

[0008]   Vsb 1 0

[0009]   M0 1 1 1 0

[0010]   .dc vsb start=min_vsb stop=max_vsb step=vsb_step

[0011]   .print lv9(m0) lx28(m0) lx29(m0)

[0012]   *Table2. Sample template 2 of HSPICE for a NMOS*

[0013]   *vds 1 0*

[0014]   *vgs 2 0*

[0015]   *m0 1 2 0 0*

[0016]   *.dc vds start=minvds stop=maxvds step=step1 vgs*

[0017]   *start=minvgs stop=maxvgs step=step2*

[0018]   *.print dc lx4(m0) lx18(m0) lx19(m0) lx20(m0)*

[0019]   *Piecewise Constant Junction capacitance Modeling*

[0020]   The value of the junction capacitance decreased monotonously as Vsb decreased, as shown at the Figure 2. According to the value of V1, there can divide the range small and large Vsb region. For convenience, let us assume the value of V1 as half of the Vmax.

[0021]   The value of capacitance Cj1 at the small Vsb region is as follows in Figure 3